Proceedings of the ASME 2009 International Design Engineering Technical Conferences & Computers and Information in Engineering Conference
IDETC/CIE 2009
October, 2021, Salt Lake City, USA

DETC2009/MESA-12345

DRAFT: REVIEW OF DESIGN AUTOMATION FOR CONTINUOUS FLOW MICROFLUIDIC CHIPS

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FLOW ROUTING

A significant focus of synthesis algorithms for flow-based microfluidic chips is in flow-routing. A small number of algorithms target naive flow routing, taking only the input of a set of control pins and generating an [optimal automated] routing path between those pins [1]. The remainder of flow-routing papers target specific applications or variations of the flow-routing problem such as obstacle-aware routing, timing-aware routing, and component-aware routing.

Obstacle-Aware Routing

Another set of fluid-routing algorithms focuses on fluid-routing for obstacle avoidance [2–5]. The typical and demonstrated most effective approach approach, introduced first by Ajwani et al. in 2011 [2] then by Huang et al. in 2013 [3], is to route the flow using a Steiner tree construction [2] and optimize the path using particle swarm optimization [3]. Steiner tree construction typically only allows for 90 degree angles, but with certain constructions, other angles such as 45 and 135 degree angles, can be allowed [4], but this demonstrates little improvement in computation time or optimal routing. Recent improvements on obstacle-avoidance algorithms have been demonstrated [5] using a Physarum-inspired (bio-inspired swarm) routing algorithm with demonstrated computational and wire-length improvement on existing algorithms such as Huang et al. 2015 [4].

Timing-Aware Routing

Additionally, some fluid-routing algorithms consider and optimize the timing and scheduling of chip operation [6, 7]. Timing constraints are added to the inputs of these algorithms in addition to the typical pin and/or obstacle constraints. Adding timing constraints improves the timing behavior of the chip resulting in an improved assay completion time, an improvement demonstrated both in simulation [7] and experimentally [6].

Component-Aware Routing

Component-aware routing algorithms as the last sub-set of flow-routing algorithms bridges the gap between flow routing and component placement, typically treated as discrete algorithmic steps, and can improve real-world performance of algorithms that are not innately physics aware. These algorithms [8–10] consider additional constrains caused by components such as valves or pumps that cannot simply be modeled as control pins. Awareness of pumps and the pressure-route constraint [10] improves timing behavior of chips by decreasing congestion. Awareness of valves and minimization of valve actuations [9] can improve reliability and chip life. Integrating the component placement and flow routing steps with sequence-pair representation of components [8] improves chip area and channel crossings in optimal routings.

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